UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/051,965 | 01/16/2002 | Shiann Liou | MP0116 | 1558 |

23624 7590 07/01/2003

MARVELL SEMICONDUCTOR, INC.
INTELLECTUAL PROPERTY DEPARTMENT
700 FIRST AVENUE, MS# 509
SUNNYVALE, CA 94089

| EXAMINER |
|---|
| THAI, LUAN C |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 07/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/051,965 | LIOU, SHIANN | |
| | Examiner | Art Unit | |
| | Luan Thai | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16 and 25-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 25-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

This Office action is responsive to the amendment filed April 08, 2003.

Claims **1-16, 25-28,** and newly added claims **29-40** are pending in this application.

Claims **17-24** have been canceled.

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first bond pad or the first *electrical termination means* (as recited in claims 1 and 9 respectively) and the second bond pad or the second *electrical termination means* (as recited in claims 6 and 14 respectively) of the at least one pair of bond pads or one pair of *electrical termination means* being *located in the internal portion of the semiconductor die* must be shown or the feature(s) canceled from the claim(s). Furthermore, "a package" as recited in claims 1, 9, 29, and 35 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

### *Claim Objections*

2. Claims **36, 37** and **39** are objected to because of the following informalities:

a) The recitations "wherein the first conducting means" in claims **36, 37** and **39**, have no antecedent basis.

b) Claim **38** is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 13. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after

allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims **1-16, 25-28** (as being amended), and newly added claims **29-40** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification, as originally filed, disclose neither "*the integrated circuit comprising an input/output (I/O) bond pad to receive an I/O bond wire operable for electrically connected to a package*", as recited in claim 1, nor "*the integrated circuit comprising an input/output (I/O) electrical termination means to receive an I/O means for conducting operable for electrically connected to a package*", as recited in claim 9. Furthermore, the specification, as originally filed, disclose neither "*the second portion of the second bond pad to receive an I/O bond wire for electrically connecting to a package*", as recited in claim 29, nor "*the second portion of the second electrical termination means to receive an I/O conducting means for electrically connecting to a package*", as recited in claim 35.

Claims **2-8, 10-16, 25-28, 30-34, and 36-40** are rejected since it includes the limitations of one of independent claims **1, 9, and 29**.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims **1-16, 25-28** (as being amended), and newly added claims **29-40,** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim **6**, the recitation "*the at least one pair of bond pads including a second bond pad located in the internal portion of the semiconductor die*" is confused with the limitation of "*a first bond pad of the at least one pair of bond pads located in an internal portion of the semiconductor die*" recited in claim **1**. Do both the first and the second bond pads of the at least one pair of bond pads *located in an internal portion* of the semiconductor die? Note that applicant's drawings do not show *both first and second bond pads* of the at least one pair of bond pads located in an internal portion of the semiconductor die.

Similarly, the recitation "*the at least one pair of electrical termination means including a second electrical termination means located in the internal portion of the semiconductor die*" in claim **14**, is confused with the limitation of "*a first electrical termination means of the at least one pair of electrical termination means located in an internal portion of the semiconductor die*" recited in claim **9**. Do both the first and the second *electrical termination means* of the at least one pair of *electrical termination means located in an internal portion* of the semiconductor die? Note that applicant's

drawings do not show *both first and second electrical termination means* of the at least one pair of *electrical termination means* located in an internal portion of the semiconductor die.

In claims **1, 9, 29, and 35**, the recitation "*for electrically connecting to a package*" is unclear as to which "a package" implies.

Claims **2-8, 10-16, 25-28, 30-34, and 36-40** are rejected since it includes the limitations of one of independent claims **1, 9, and 29**.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 29-31 and 33-35, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 102(e) as being anticipated by Schoenfeld (6,348,400).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 29-31 and 33-35, Schoenfeld (see specifically figures 6A-6B attached) disclose an integrated circuit comprising: a semiconductor die (20) including a pairs of electrical termination means (e.g., bond pads A/B), a first electrical termination means (e.g., bond pads A) of the pair of electrical termination means (e.g., bond pads

A/B) located in an internal portion of the semiconductor die (20) and having a first end of a first conducting means (e.g., a first bond wire 34) connected thereto, a second electrical termination means (e.g., bond pads B) of the pair of electrical termination means (e.g., bond pads A/B) located in a periphery of the semiconductor die (20) and having a first portion (B2) and second portion (B1), the first portion (B2) having a second end of the first conducting means (e.g., the first bond wire 34) connected thereto, the second portion (B1) to receive an I/O conducting means (e.g., bond wire 32) for electrically connecting to a package. Schoenfeld further discloses the first bond wire (34) made of a metallic material selected from the group consisting of gold and aluminum (Col. 4, lines 37+), and bonded to the pair of bond pads (A/B) using ball bonds or stitch bonds on ball (Col. 4, lines 30+). Although Schoenfeld does not explicitly disclose the first bond wire being selected from the group consisting of power interconnect, ground interconnect, and signal interconnect, this feature is taken to be inherent in Schoenfeld integrated circuit, since the first bond wire being electrically connected to the bond pads is disclosed and it would be that the bond wire must be one of power interconnect, ground interconnect, or signal interconnect, for the integrated circuit to function as intended.

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-2, 6-10, 14-16, 26, and 39-40, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar et al (5,495,398).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-2, 6-10, 14-16, 26, and 39-40 Takiar et al disclose (see specifically figures 5-6 attached) an integrated circuit comprising: a semiconductor die (158) including a plurality of pairs of electrical termination means (e.g., bond pads A/B) and electrical termination means (e.g., bond pads C) connected to the connecting means (e.g., lead fingers 168); each pair of electrical termination means (e.g., bond pads A/B) having a single corresponding means (e.g., bond wire X) connected thereto such that each electrical termination means (e.g., bond pads A/B) of the pair of electrical termination means has only one end of any means (e.g., one bond wire end) for conducting connected thereto, wherein the first and the second electrical termination means (e.g., bond pads A and B) are located in the internal portion of the semiconductor die (158), and wherein the single corresponding means (e.g., bond wire X) would inherently be one of power interconnect, ground interconnect, or signal interconnect. Takiar et al further disclose the second electrical termination means (e.g., the second bond pad B) being located along a periphery of the semiconductor die (158) (see figure 6).

Although Takiar et al do not explicitly disclose the electrical termination means (e.g., bond pads C) being I/O electrical termination means (or I/O bond pad), it would have been obvious for at least one of lead finger (168), which is electrically connected to the electrical termination means (e.g., bond pads C) via bond wire (Y), to be an

input/output lead operable for electrically connecting to a package, for the integrated circuit to function as intended.

11. Claims 3-4, 11-12 and 36-37, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar et al (5,495,398) in view of Schoenfeld (6,348,400).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 3-4, 11-12 and 36-37, the proposed integrated circuit of Takiar et al discloses all the limitations of the claimed invention as detailed above except for specifying the material making the single corresponding means or bond wire (e.g., gold, aluminum, or copper) and the bonding technique (e.g., ball bonds, stitch bonds, stitch bonds on bonding pad, or stitch bonds on ball).

Schoenfeld while related to a similar wire bonding for a semiconductor device teaches the bonding wire being made of gold or aluminum, and the bonding technique being ball bonds or stitch bonds (Col. 4, lines 31+ and lines 38+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use gold or aluminum for making the bond wire and ball bonds technique for connecting the bond wire to the bond pads in Takiar et al's device, since such material (e.g., gold and aluminum) and such bonding technique (e.g., ball bonds and stitch bonds) are commonly applied in semiconductor art, as taught by Schoenfeld.

12. Claims 5, 13, and 38, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar et al (5,495,398) in view of Manning et al. (6,169,331 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 5, 13, and 38, the proposed integrated circuit of Takiar et al discloses all the limitations of the claimed invention as detailed above except for a trace in the semiconductor die connected between the pair of bond pads (e.g., electrical terminal means).

Manning et al. while related to a similar integrated circuit die design teach (see specifically figure 3A) a pair of bond pads 121a-121b are connected together not only by bond wire 150b (outside the semiconductor die 120) but also by the trace 153 (inside the semiconductor die 120) in order to reduce electrical resistance between the two bond pads 121a-121b (Col. 4, lines 59+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takiar et al's integrated circuit by forming an additional trace in the semiconductor die connected between the pair of bond pads (e.g., electrical terminal means), as taught by Manning et al., in order to reduce electrical resistance between the two bond pads (e.g., electrical terminal means), and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

13. Claim 32, insofar as in compliance with 35 USC § 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Schoenfeld (6,348,400) in view of Manning et al. (6,169,331 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 32, Schoenfeld discloses all the limitations of the claimed invention as detailed above except for a trace in the semiconductor die connected between the pair of bond pads.

Manning et al. while related to a similar integrated circuit die design teach (see specifically figure 3A) a pair of bond pads 121a-121b are connected together not only by bond wire 150b (outside the semiconductor die 120) but also by the trace 153 (inside the semiconductor die 120) in order to reduce electrical resistance between the two bond pads 121a-121b (Col. 4, lines 59+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schoenfeld's integrated circuit by forming an additional trace in the semiconductor die connected between the pair of bond pads, as taught by Manning et al., in order to reduce electrical resistance between the two bond pads, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

***Conclusion***

14. Applicant's arguments with respect to claims **1-16, 25-28,** and newly added claims **29-40** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the changes (e.g., the underlined portions) in claims 1, 5, 9, 13 and newly added claims 29-40 raise new issues that would require further consideration and/or search. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

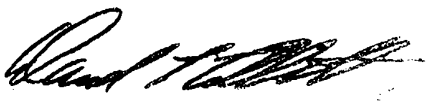
16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
June 28, 2003



DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

(Attachment)



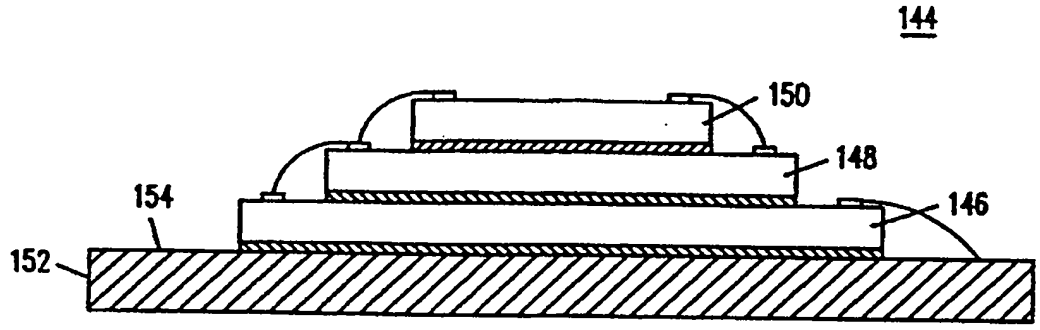



FIG. 5

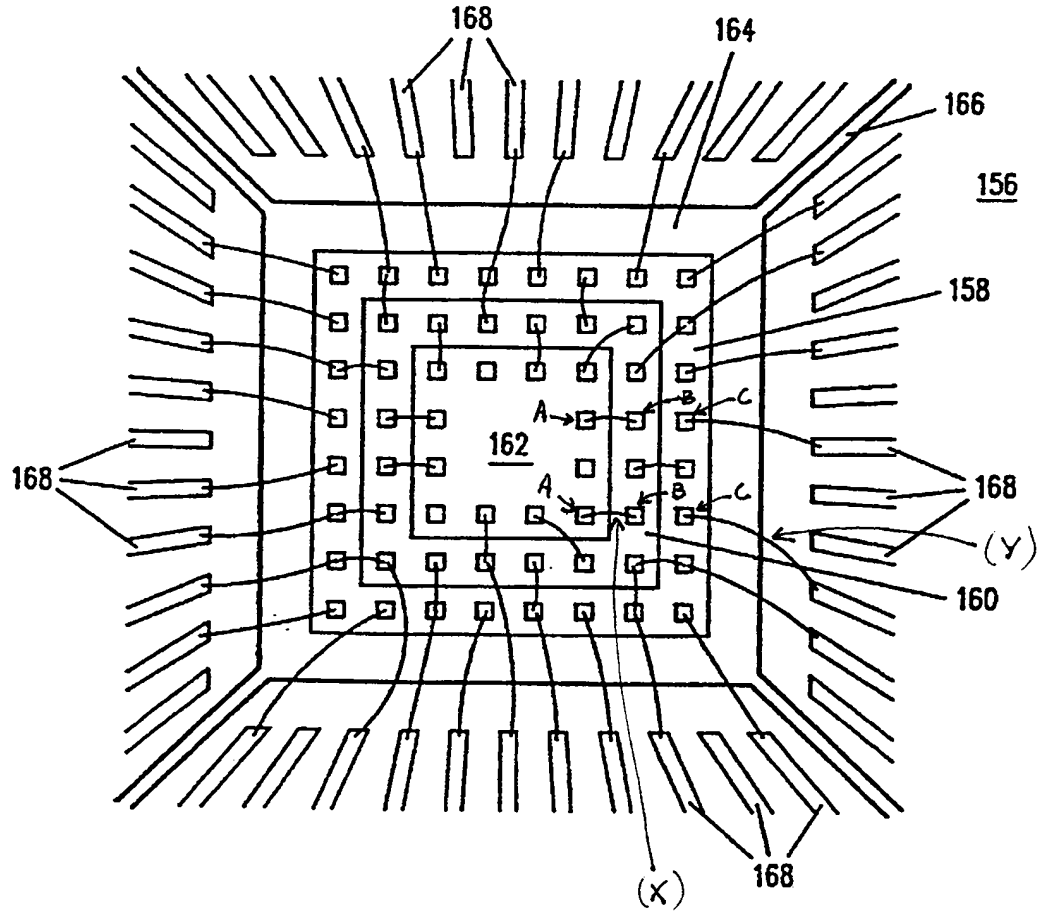



FIG. 6

(Attachment)



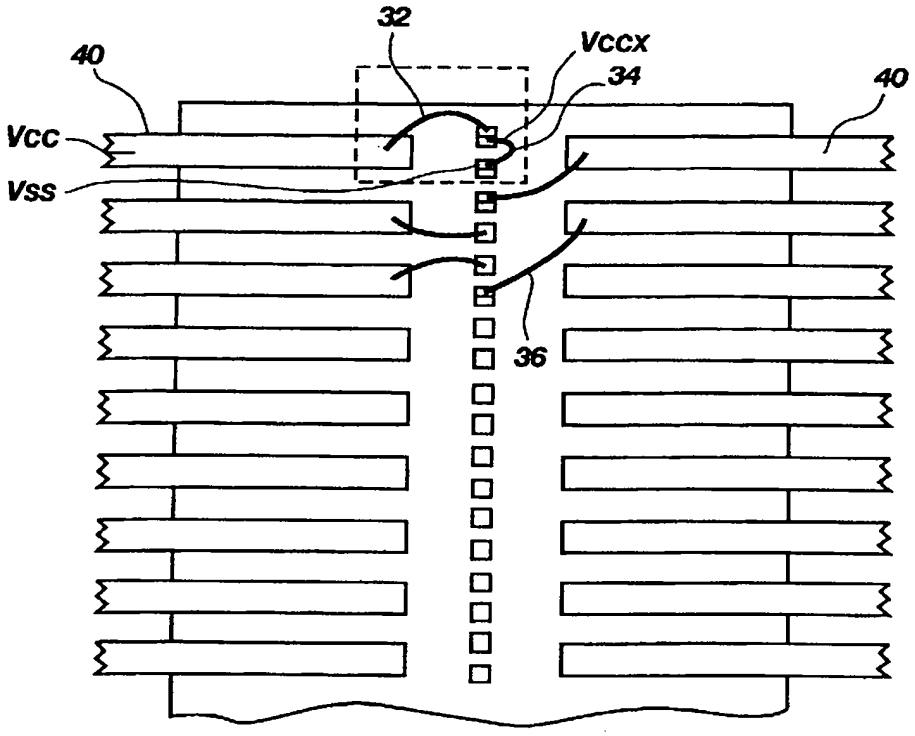



Fig. 6A

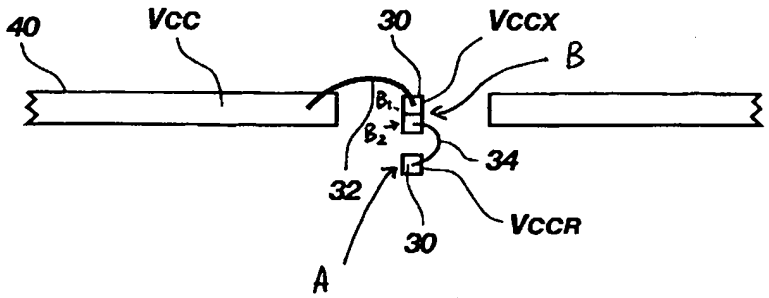



Fig. 6B